DYNAMIC CLOCK GENERATOR WITH RISING EDGE ALIGNMENT ENABLE SIGNAL

ABSTRACT OF THE DISCLOSURE

A method and apparatus for providing a dynamically alterable output clock from an input clock based on the value of an integer, where the integer can be modified continuously. The invention also provides a sample cycle output which is an enable pulse, having the width of the input clock cycle, that is asserted one or two input clock cycles prior to the rising edge alignment of the input and output clocks, that acts as a rising edge alignment enable signal, maintaining a one-to-one correspondence between the sample cycle assertions and rising edge alignment events, regardless of the dynamic changes in the value of the integer.